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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,645	11/21/2003	Jonathan H. Fischer	46-3	1260

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EXAMINER	
RODRIGUEZ, GLENDA P	

ART UNIT	PAPER NUMBER
2651	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,645	FISCHER ET AL.	
	Examiner	Art Unit	
	Glenda P. Rodriguez	2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Horie et al. (US Patent No. 6, 054, 887).

Regarding Claim 1, Horie et al. teaches a sample and hole circuit having an input and output, comprising:

At least one capacitive element for retaining a charge, said at least one capacitive element connected to a node between said input and said output (Element 14 in Fig. 10, wherein it teaches the capacitor being connected between the input and output of the given circuit.);

At least one input switch for selectively connecting said at least one capacitive element to said input (Elements 5 and 26 of Fig. 10);

At least one output switch for selectively connecting said at least one capacitive element to said output (Switches 22 and 24 of Fig. 10 are the output switches to the output, which is the DAC element as disclosed in Col. 6, L. 21-33);

And an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage (Element 1 in Fig. 10).

Method claim (8) is drawn to the method of using the corresponding apparatus claimed in claim (1). Therefore method claim (8) corresponds to apparatus claim (1) and is rejected for the same reasons of anticipation as used above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4 and 10, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horie et al. in view of Beauducel et al (US Patent No. 4, 352, 070).

Regarding Claims 3 and 10, Horie et al. teaches all the limitations of Claims 1 and 8. However, Horie et al. does not explicitly teach wherein at least one of said input and output switches has a leakage effect represented by a resistor in parallel with said input or output switch and a voltage drop across said resistor is limited to said offset voltage. Beauducel et al. does teach a resistor placed in parallel as disclosed in the sample and hold circuit of Fig. 4, Resistor R_1. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Horie et al.'s invention with the teaching of Beauducel et al. in order to provide a passive compensation to the circuit (Col. 1, L. 65-67 of Beauducel et al.).

Regarding Claims 4 and 11, Horie et al. teaches all the limitations of Claims 1 and 8. However, Horie et al. does not explicitly teach wherein further comprising at least two switches associated with at least one of said input and output switches, wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier in a hold mode or standard voltages in a write mode to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches. Beauducel et al. teaches two switches found between the input and output nodes in order to hold a voltage amount (See Col. 3, L. 1-20 of Beauducel et al.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Horie et al.'s invention with the teaching of Beauducel et al. in order to provide a passive compensation to the circuit (Col. 1, L. 65-67 of Beauducel et al.).

Regarding Claims 7 and 13, Horie et al. teaches all the limitations of Claims 1 and 8, respectively. However, Horie et al. does not distinctively teach wherein at least one of the switches reduces leakage in the sample and hold circuit. Beauducel et al. teaches at least one of the switches reduces leakage in the sample and hold circuit in Col., L. 1-20 in order to control the voltage amount. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Horie et al.'s invention with the teaching of Beauducel et al. in order to provide a passive compensation to the circuit (Col. 1, L. 65-67 of Beauducel et al.).

Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horie et al. in view of Mills et al. (US Patent No. 5, 172, 117). Horie et al. teach all the limitations of Claims 1 and 8, respectively. However, Horie et al. does not explicitly teach wherein the hold

time is 200 microseconds. Mills et al. teaches a sample and hold circuit in which its hold time is 200 microseconds (Col. 4, L. 35-40 of Mills et al.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Horie et al.'s invention with the teaching of Mills et al. in order to acquire a precise data acquisition (Col. 2, L. 45-50 of Mills et al.).

Claims 2, 5, 9, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horie et al. in view of Sandusky et al. (US Patent No. 5, 825, 571).

Claim (14) have limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claims (14) however also recites the following limitations..."a magneto resistive head in a disc drive". However, Horie et al. does not explicitly teach wherein the sample and hold circuit is for a disc drive. Sandusky et al. teaches a sample and hold circuit for a preamplifier in a disk drive apparatus (Col. 6, L. 6-24). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Horie et al.'s invention with the teaching of Sandusky et al. in order to inhibit AC transients (See Abstract Sandusky et al.).

Regarding Claims 2, 5, 9 and 15, Horie et al. teach the limitations of Claims 1 and 8, respectively. However, Horie et al. does not explicitly teach wherein the sample and hold circuit is for a disc drive. Sandusky et al. teaches a sample and hold circuit for a preamplifier in a disk drive apparatus (Col. 6, L. 6-24). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Horie et al.'s invention with the teaching of Sandusky et al. in order to inhibit AC transients (See Abstract Sandusky et al.).

Claims 16, 17, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horie et al. and Sandusky et al. as applied to claim 14 above, and further in view of Beauducel et al. (US Patent No. 4, 352, 070).

Regarding Claims 16, the combination of Horie et al. and Sandusky et al. teaches all the limitations of Claim 14. However, Horie et al. does not explicitly teach wherein at least one of said input and output switches has a leakage effect represented by a resistor in parallel with said input or output switch and a voltage drop across said resistor is limited to said offset voltage. Beauducel et al. does teach a resistor placed in parallel as disclosed in the sample and hold circuit of Fig. 4, Resistor R_1. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the combination's invention with the teaching of Beauducel et al. in order to provide a passive compensation to the circuit (Col. 1, L. 65-67 of Beauducel et al.).

Regarding Claims 17, the combination of Horie et al. and Sandusky et al. teaches all the limitations of Claim 14. However, Horie et al. does not explicitly teach wherein further comprising at least two switches associated with at least one of said input and output switches, wherein said at least two switches selectively connect at least one of said input and output switches to an output of said amplifier in a hold mode or standard voltages in a write mode to reduce leakage effects due to parasitic diodes in said at least one of said input and output switches. Beauducel et al. teaches two switches found between the input and output nodes in order to hold a voltage amount (See Col. 3, L. 1-20 of Beauducel et al.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the

combination's invention with the teaching of Beauducel et al. in order to provide a passive compensation to the circuit (Col. 1, L. 65-67 of Beauducel et al.).

Regarding Claim 20, the combination of Horie et al. and Sandusky et al. teaches all the limitations of Claim 14. However, Horie et al. does not distinctively teach wherein at least one of the switches reduces leakage in the sample and hold circuit. Beauducel et al. teaches at least one of the switches reduces leakage in the sample and hold circuit in Col., L. 1-20 in order to control the voltage amount. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the combination's invention with the teaching of Beauducel et al. in order to provide a passive compensation to the circuit (Col. 1, L. 65-67 of Beauducel et al.).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horie et al. and Sandusky et al. as applied to claim 14 above, and further in view of Mills et al. (US Patent No. 5, 172, 117). The combination of Horie et al. and Sandusky et al. teach all the limitations of Claims 1 and 8, respectively. However, Horie et al. does not explicitly teach wherein the hold time is 200 microseconds. Mills et al. teaches a sample and hold circuit in which its hold time is 200 microseconds (Col. 4, L. 35-40 of Mills et al.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the combination's invention with the teaching of Mills et al. in order to acquire a precise data acquisition (Col. 2, L. 45-50 of Mills et al.).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (571) 272-7561. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on (571) 272-7843. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gpr
July 5, 2005.

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